REMARKS

The Examiner's Action mailed on March 25, 2005 has been received and its contents carefully considered. Additionally attached to this Amendment is a petition for extension of time, extending the period for response to August 25, 2005.

In this Amendment, Applicants have amended claims 25-30 and 47-50. Claims 51-52 are added to further protect the invention. Claims 25 and 47 are the independent claims. Claims 25-30, 47-50 and 51-52 are now pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 25-26 and 47-49 have been rejected under 35 U.S.C. 102(b) as being anticipated by *Hamzehdoost et al.* (U.S. Patent No. 5,689,091). Claims 25 and 47 have been amended, and it is submitted that the rejection is inapplicable to the amended claims 25 and 47 and their dependent claims 26 and 48-49.

It is well settled that a reference may anticipate a claim within the purview of 35 USC section 102 only if all the features and all the relationships recited in the claim are taught by the reference structure either by clear disclosure or under the principle of inherency.

Applicants' independent claim 25 recites a method of manufacturing a coaxial via hole structure, including: (a) forming a first hole in a carrier; (b) making the interior of the first hole conduct electricity to form an outer cylinder-shaped conductor; (c) placing a **high-dielectric-constant material** in the outer cylinder-

shaped conductor to form a high-dielectric-constant region; (d) forming a second hole in the high-dielectric-constant region, wherein the second hole has a diameter smaller than the diameter of the first hole; and (e) making the interior of the second hole conduct electricity to form an inner cylinder-shaped conductor. The coaxial via hole structure serves as a capacitor.

In contrast, Hamzehdoost et al. disclose a multi-layer substrate structure and a method of fabricating the same. The multi-layer substrate structure has a cavity to receive an IC die and a plurality of plated-through holes formed by a conductive metal layer 20, an epoxy 22 and a conductive metal layer 30. First, holes 16 formed in the copper laminate substrate 14 are deposited with a conductive metal layer 20 and then filled with an epoxy 22. After that, holes 26a are formed within the epoxy-filled holes and then plated with a conductive metal layer 30. The conductive metal layer 30 and the conductive metal layer 20 respectively have wire bondable areas 34 and solderable areas 36. In the die bonding process, one ends of the bonding wires 40 are bonded to the IC die 38 and other ends are bonded to the solderable areas 36. Solder balls 44 are attached to the solderable areas 36 in order to form the completed IC chip package 110 (Col. 3, lines 19-50).

However, the plated through holes in substrate 14 of *Hamzehdoost et al.* are simply used for signal transmission in the IC chip package. This contrasts with the claimed invention in which the coaxial via hole structure serves as a capacitor.

Further, there is no disclosure (or even a suggestion) by *Hamzehdoost et al.* of a high-dielectric-constant region formed between the outer cylinder-shaped conductor and the inner cylinder-shaped conductor, as recited in claim 25. Rather, the epoxy 22 of *Hamzehdoost et al.* is not a material with a high-dielectric constant.

Therefore, it is submitted that Applicant's independent claim 25, as well as claim 26 dependent therefrom, are not anticipated by (or rendered obvious by) the cited reference.

Further, Applicants' independent claim 47 recites a method of manufacturing a coaxial via hole structure, including: (a) forming a first hole in a carrier; (b) making the interior of the first hole conduct electricity to form an outer cylinder-shaped conductor; (c) placing an **electrical-resistant material** in the outer cylinder-shaped conductor to form an electrical-resistant region; (d) forming a second hole in the electrical-resistant region, wherein the second hole has a diameter smaller than the diameter of the first hole; and (e) making the interior of the second hole conduct electricity to form an inner cylinder-shaped conductor. The coaxial via hole structure serves as **a resistor**.

In contrast, the plated through holes in substrate 14 of *Hamzehdoost et al.* are simply used for signal transmission in an IC chip package. This contrasts with the claimed invention in which the coaxial via hole structure serves as a resistor.

Further, there is no disclosure (or even a suggestion) by *Hamzehdoost et al.* of an electrical-resistant region formed between the outer cylinder-shaped

conductor and the inner cylinder-shaped conductor, as recited in claim 47. Instead, the epoxy 22 of *Hamzehdoost et al.* is not an electrical-resistant material.

Therefore, it is submitted that Applicants' independent claim 47, as well as the claims 48-49 dependent therefrom, are not anticipated by (or rendered obvious by) the cited reference. It is therefore requested that this rejection be withdrawn.

Claims 25-27, 29-30 and 47-49 have been rejected under 35 U.S.C. 102(b) as being anticipated by *Fasano et al.* (U.S. Patent No. 5,949,030). Claims 25 and 47 have been amended, and it is submitted that the rejection is inapplicable to the amended claims 25 and 47 and their dependent claims 26-27, 29-30 and 48-49.

Fasano et al. disclose vias and a method for making the same in organic board and chip carriers. Multiple vias are produced coaxially or in axis parallel alignment in a first or primary through-hole in a printed circuit board, chip carrier or like electrical device by producing a primary metallized through hole or via which is then filled or coated with a dielectric material which is also placed on both surfaces of the device at the ends of the via (Abstract; and FIG. 3).

Multiple vias provide a conductive path from the top surface 14 to the bottom surface 16 of the device 10 (Col. 3, lines 64-67). That is, multiple vias of *Fasano et al.* are simply used for signal transmission in the device 10. This contrasts with the claimed invention in which the coaxial via hole structure serves as a capacitor, as recited in claim 25, and in which the coaxial via hole structure serves as a resistor, as recited in claim 47.

Further, there is no disclosure (or even a suggestion) by *Fasano et al.* of a high-dielectric-constant region formed between the outer cylinder-shaped conductor and the inner cylinder-shaped conductor, as recited in claim 25. Moreover, there is no disclosure (or even a suggestion) by *Hamzehdoost et al.* of an electrical-resistant region formed between the outer cylinder-shaped conductor and the inner cylinder-shaped conductor, as recited in claim 47.

Therefore, it is submitted that Applicants' independent claims 25 and 47, as well as the claims 26-27, 29-30 and 48-49 dependent therefrom, are not anticipated by (or rendered obvious by) the cited reference. It is therefore requested that this rejection be withdrawn.

Claims 28 and 50 have been rejected under 35 U.S.C. 103(a) as being unpatentable over *Hamzehdoost et al.* in view of *Bhatt et al.* (U.S. Patent No. 5,487,218). Independent claims 25 and 47 have been amended. Claims 28 and 50 respectively depend from claims 25 and 47. The cited secondary reference of *Bhatt et al.* fails to disclose or even suggest the features recited in claims 25 and 47 missing from *Hamzehdoost et al.* Therefore, claims 28 and 50 are patentable

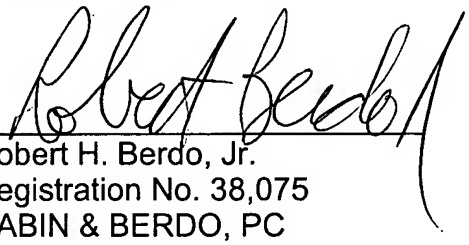
over the cited references for at least the reasons advanced above as to the patentability of independent claims 25 and 47. The rejection accordingly should be withdrawn.

Based on the above, it is submitted that this application is in condition for allowance and such a Notice, with allowed claims 25-30 and 47-52, earnestly is solicited.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Should the remittance be accidentally missing or insufficient, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,



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Date

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